said element selection logic means portion for causing the instruction to be executed by those said elements which perform those associated said logical sequences affecting the instruction execution in an optimum manner including means for transmitting and switching signals to said elements optically.

REMARKS

The pending claims are 1-4, 11, 12, 19-22 and 37-41. New claims 39-41 added by this amendment reinstate previously cancelled claims 5, 13 and 23, respectively. Claims 6-10, 14-18 and 24-36 were withdrawn from consideration following a restriction requirement. It is the applicant's understanding that "If claims 1-5 are subsequently found to be allowable, the question of rejoinder will be considered."

DISCUSSION OF THE CITED REFERENCES

McAulay is incompatible with selecting among plural execution means on a per-instruction basis:

McAulay's system can only reconfigure its crossbar switch (connected to plural execution logic units) prior to execution of a user's ALGORITHM comprising many instructions and cannot reconfigure during the execution of the algorithm to customize itself for each instruction. This is because McAuley configures his crossbar switch from a directed graph of the algorithm mapped to the crossbar switch in such a manner as to guarantee maximum parallelism. See McAuley column 10 line 62 through column 11 line 7. In many cases, McAuley's goal of mapping the entire algorithm onto the crossbar switch for maximum parallelism will be inconsistent with or prevent the realization of the goal of the Applicant's invention of optimizing the execution of EACH INSTRUCTION. In any case, McAuley has nothing to do with reconfiguring plural instruction execution means (e.g., processors) with the execution of each individual instruction.

Brown has nothing to do with configuring plural processors:

Brown is simply a priortization system for a single processor to handle multiple interrupt requests. For this very limited purpose, Brown teaches classifying individual interrupt requests or instructions, but only for the purpose of deciding which interrupt to handle next (using the SAME processor to handle all such interrupts). Brown has nothing to do with the subject matter of McAuley --nor for that matter of the present invention--, namely the execution of user ALGORITHM instructions. Brown is concerned only with operating system management tasks of prioritizing among a plurality of system-generated interrupts, arising for example from system use by multiple users or different functions. Such operating system management tasks have nothing to do with the problem solved by the present invention of optimizing the execution of each user instruction.

The combination of McAuley with Brown would not lead to Applicant's invention:

The combination suggested in the Office Action is to place the device of Brown within or in place of McAuley's controller 46. First, the result would be non-functional, because Brown's device can only prioritize among many interrupts for handling by a single processor, which is incompatible with the function of McAuley requiring maximum parallelism among plural processors and requires execution of a user algorithm, not merely interrupt requests. Thus, the combination would not function. Secondly, the combination, if it did somehow function, could only meet the functional goals of McAuley and Brown, which is a system --per McAuley-- configured among plural processors prior to algorithm execution to maximize parallelism for THAT ALGORITHM (regardless of optimizing individual instruction execution) and --per Brown--a system with neatly arbitrates among competing interrupt

requests to a single processor. Such a combination hardly begins to suggests the present Applicant's invention of optimally reconfiguring plural processors for each user instruction DURING ALGORITHM EXECUTION.

Wherefore, in view of the foregoing amendment and these remarks, it is applicant's belief that this application is now in condition for allowance and for the rejoinder of the withdrawn claims. Re-examination and rejoinder is respectfully requested and, in the absence of newly cited art, favorable reconsideration in the form of an early Notice of Allowance is courteously solicited.

An extension of time of two months extending the time for response from 5 June 1990 to 5 August 1990 is requested and petitioned for. Because 5 August 1990 falls on a Sunday, the actual time for response will therefore be 6 August, 1990. The required fee of $ 90.00 (Fee Code 216) is enclosed herewith.

Respectfully submitted,

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I certify that the foregoing was mailed by First Class Mail with postage attached and addressed to the Hon. Commissioner of Patents & Trademarks, Washington, DC 20231 on 6 August 1990.

Donald A. Streck

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